IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 7, Issue 1, January 2018

# Design and Optimization Low Power Adder using GDI Technique

**Dolly Gautam[1], Mahima Singh[2], Dr. S. S. Tomar[3]**

M.Tech. Students, Department of ECE, MPCT College, Gwalior, Madhya Pradesh, India[1-2]

Associate Professor, Department of ECE, MPCT College, Gwalior, Madhya Pradesh, India[3]

**Abstract:** The main objective of this paper is to provide new low power solutions for Very Large Scale Integration (VLSI) Designers. This works focuses on power dissipation reduction. Due to which growth increases with the scaling down of the technologies. Addition is a fundamental arithmetic operation widely used in many VLSI systems, such as application specific DSP architectures and microprocessors. The adder is one of the most critical components of a central processing unit. The object of the adders not only adding of bits but also involves in address calculation, subtraction, division and multiplication, the adders are critical components to determine the speed, delay and power of the overall system, low power adders are always preferable.

**Keywords:** Adder, GDI, Low Power VLSI, Leakage current.

## I Introduction

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operator, and similar operations.[1]

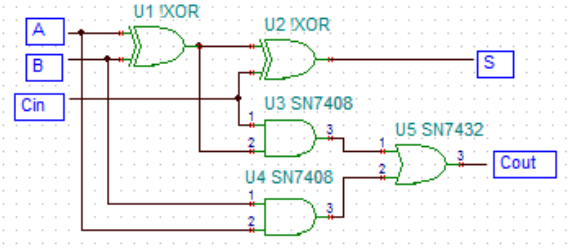


Fig 1 Adder cell

## II FOUR BIT RIPPLE CARRY ADDER

A simple ripple carry adder (RCA) is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Inter connection of four full adder circuits to provide a four bit ripple carry adder. Notice from Fig. 2 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a0 and b0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits S0 – S3. The main problem with this type of adder is the delays needed to produce the carry out signal and the most significant bit [2]. These delays increase with the increase in the number of bits to be added

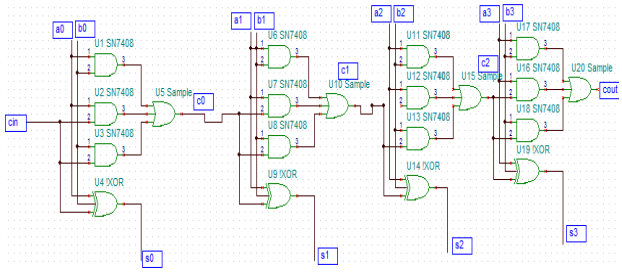


Fig 2 ripple carry Adder

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319-5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 7, Issue 1, January 2018

## III FOUR BIT CARRY LOOK AHEAD ADDER

The carry look-ahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases: (1) when both bits a and b are 1, or (2) when one of the two bits is 1 and the carry-in is 1.

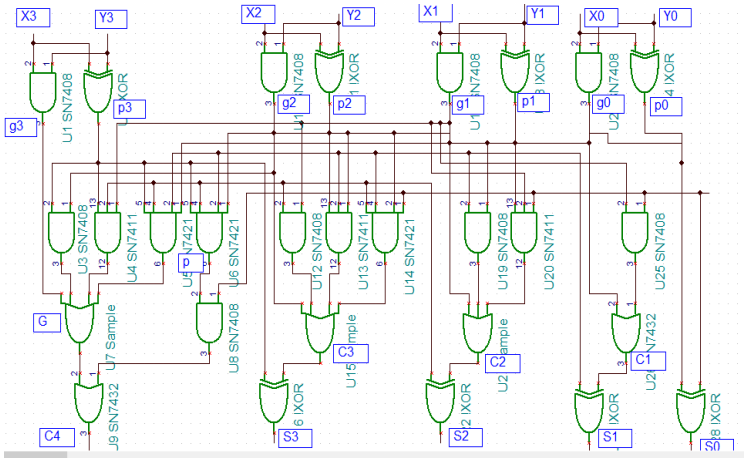


Fig 3 carry look ahead Adder

## IV LEAKAGE POWER

Leakage power, also called static power, is due to the off-state current of a when it is off. Suppose that there are N transistors in a circuit, and Ioffi is the off-state current transistor of the ith transistor. Leakage power Leakage power is the power consumed by a device not related to state changes . Leakage power is actually consumed when a device is both static and switching, but generally the main concern with leakage power is when the device is in its inactive state, as all the power consumed in this state is considered “wasted” power . Different causes for the leakage power like reverse bias current, sub threshold channel leakage current, drain induced barrier lowering leakage, gate induced drain leakage, punch through, narrow width effect, gate oxide tunneling current, and hot carrier injection current

## V GDI TECHNIQUE

Gate Diffusion Input (GDI) is a technique for designing low power circuits. This technique allows usage of less number of transistors as compared to CMOS logic. The basic GDI cell consists of only two transistors which are used to implement the basic logic functions. Because of less number of transistors, the switching is reduced and hence there will be a less power, delay and also reduced area.

## VI LOGIC OF GDI TECHNIQUE

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and low power circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top- down approach by means of small cell library.

The GDI functions given as I is simply the extension of a single input CMOS inverter structure into a triple input GDU cell in order to achieve implementation of complicated logic functions with a minimal number of transistors. Extension of any n-input CMOS structure to an (n+ 2) input GDI cell can be done by using P as input instead of supply voltage in the pMOS block of a CMOS structure and an N input instead of ground in the nMOS block. This extended implementation can be represented by the following logic expression :

Out = F’(x1……..xn)P + F(x1……..xn)N

Where *F( x1…….xn)* is a logic function of an nMOS block not of the whole original n-input CMOS structure. The above equation is based on Shannon expansion, where any function *F* can be written as follows:

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 7, Issue 1, January 2018

F(x1.....xn) = x1 H(x2……...xn) + x1' G(x2…....xn)
= x1 F (1,x2…..xn) + x1' F(0,x2....xn)
The output functions of basic GDI cell are based on Shannon expansion where A, B and C are inputs to G, P and N respectively as,
OUT = AC + A'B

## VII METHODOLOGY FOR GDI

GDI technique has analyzed by designing basic digital gates and few combinational circuits such as ripple adder, carry looks ahead full adder and comparator for 4 bit binary numbers at 180nm technology using CADENCE EDA VLSI TOOL. The performance of GDI is also measured in high level digital combinatorial circuits. For analysis purpose half adder, full adder, ripple adder, carry look ahead adder and comparator were also implemented using GDI and CMOS design techniques. Half Adder and Full adder are designed using XOR, AND and OR gate combination

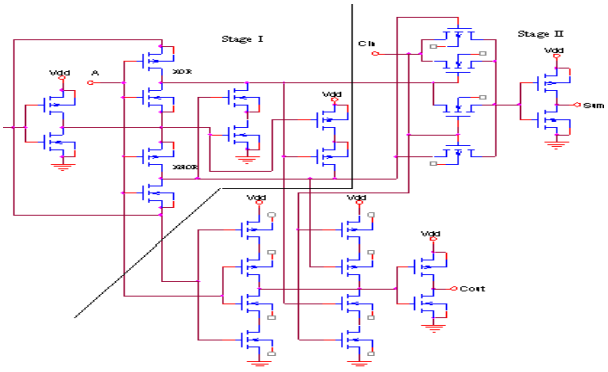


Fig 4 GDI XOR/XNOR Adder

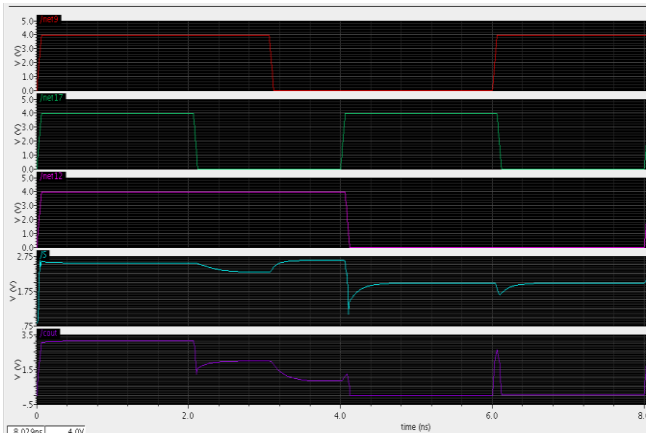

Fig 5 Output wave form

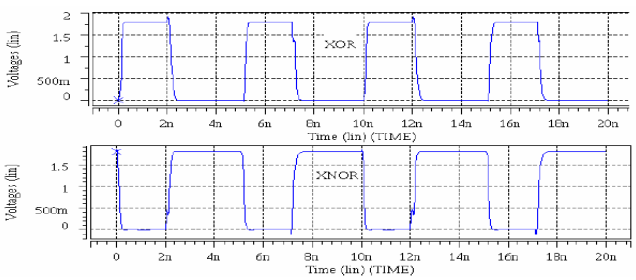


Fig 6 Output transient response XOR XNOR

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 7, Issue 1, January 2018

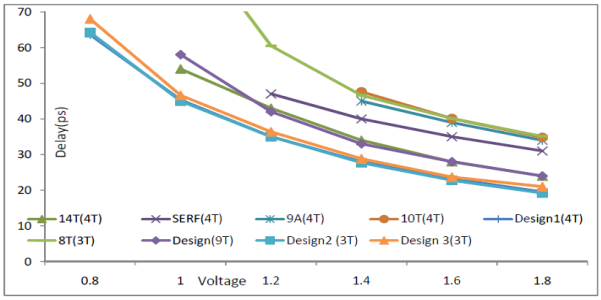


Fig Delay comparison of full adder

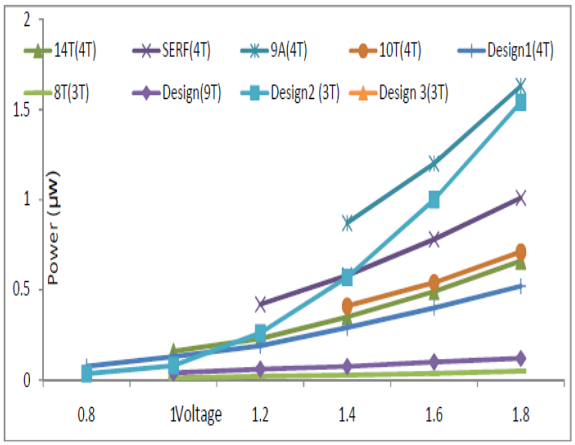


Fig Power (uW) comparison of full adder

Table 1 Power vs Supply Volatge

| Logic Style | Power Vs Supply Voltage (Absolute Power (mWatt) and *Normalized Power (mWatt/MHz)* | | | | | |
|---|---|---|---|---|---|---|
| | 5V | 4.5V | 4V | 3.5V | 3V | 2.5V |
| CMOS | 21.5 (1.72) | 15.5 (1.55) | 6.0 (1.5) | 5.3 (1.33) | 4.8(1.2) | 2.8(0.7) |
| GDI | 15.2 (1.22) | 9.8 (0.98) | 3.3 (0.83) | 3.1 (0.78) | 2.9(0.73 ) | 2.5(0.63) |

Table 1 Delay vs Supply Volatge

| Logic Style | Delay (nsec) Vs Voltage supply | | | | |
|---|---|---|---|---|---|
| | 5V | 4V | 3.5V | 3V | 2.5V |
| CMOS | 76 | 100 | 117 | 154 | 235 |
| GDI | 76 | 100 | 116 | 153 | 233 |

## REFERENCES

[1]. Pattanaik, M.; Khan, F.R.; Varaprasad, M.V.D.L. Enhanced Ground Bounce Noise Reduction in a Low Leakage 90nm 1-Volt CMOS Full Adder Cell Electronic Devices, Systems and Applications (ICEDSA), 2010 Intl Conf on Year: 2010.

[2]. Jaramillo-Ramirez, R.; Anis, M. "A Dual-Threshold FPGA Routing Design for Subthreshold Leakage Reduction" Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on Year: 2007

[3]. Gala, N.; Devanathan, V.R.; Srinivasan, K.; Visvanathan, V.; "ProCA: Progressive Configuration Aware Design Methodology for Low Power Stochastic ASICs" VLSI Design and 2014 13th International Conference on Embedded Systems, 2014 27th International Conference on Year: 2014

[4]. Shrivastava, A.K.; Akashe, S. Design high performance and low power 10T full adder cell using double gate MOSFET at 45nm technologyControl Computing Communication & Materials (ICCCCM), 2013 International Conference on Year: 2013

[5]. Pable, S.D.; Imran, A.; Hasan, M. "Performance optimization of CNFET based subthreshold circuits" India Conference (INDICON), 2010 Annual IEEE Year: 2010

[6]. Tajalli, A.; Leblebici, Y. "Design Trade-offs in Ultra-Low-Power Digital Nanoscale CMOS" Circuits and Systems I: Regular Papers, IEEE Transactions on Year: 2012

[7]. Ghafari, P.; Anis, M.; Elmasry, M. Impact of technology scaling on leakage reduction techniques Circuits and Systems, 2007. NEWCAS 2007. IEEE Northeast Workshop on Year: 2007

[9]. U. Supriya, K. Ramana Rao "Design of Low Power CMOS Circuits using Leakage Control Transistor and Multi-Threshold CMOS Techniques",Int.J.Computer Technology & Applications,Vol 3 (4), 1496-1500

[10]. Namrata Gupta "Designing of Full Adder Circuits for Low Power" International Journal of Scientific Research Engineering & Technology (IJSRET) Volume 2 Issue4 pp 215-219 July 2013

[11]. Mrs. Sujatha Hiremath, Dr. Deepali Koppad " Low Power Circuits using Modified Gate Diffusion Input (GDI)" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 5, Ver. II (Sep-Oct. 2014).